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a first nitride spacer formed on the oxide layer;
a second nitride spacer formed on the oxide layer;
lightly doped drain (LDD) regions formed in the active region of the semiconductor substrate on both sides of the gate electrode;
source/drain regions formed in the active region of the semiconductor substrate on both sides of the gate electrode; and
second and third insulating films filling and planarizing the space above the active region and between the gate electrode structure and the second nitride spacer.

2. (Amended) The transistor according to claim 1, wherein the groove has a rounded profile near the junction of the device isolation film and the semiconductor substrate.

3. (Amended) The transistor according to claim 1, further comprising a hard mask layer on the gate electrode structure.

See the attached Appendix for the changes made to effect the above claim(s).